WHAT IS CLAIMED IS:

1. A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said central processing unit and to said IOP, and means for arbitrating access of said central processing unit and said IOP to said global memory unit.

2. The microprocessor system of claim 1 in which said global memory unit comprises a plurality of global registers.

3. The microprocessor system of claim 1 wherein said central processing unit includes an arithmetic logic unit and a push-down stack coupled to said arithmetic logic unit.

4. The microprocessor system of claim 1 further including a memory interface unit coupled to said global memory unit, to said microprocessing unit, and to said IOP.

5. The microprocessor system of claim 4 further including a means for arbitrating access of said memory interface unit and said microprocessing unit to said global memory unit.

6. The microprocessor system of claim 5 additionally comprising a system memory and at least one input-output device coupled to said memory interface unit and wherein each storage location in said global memory unit holds a single address comprised of a first grouping of address bits coupled to address said system memory and a second grouping of address bits coupled to address said at least one input-output device.

7. The microprocessor system of claim 5 additionally comprising a system memory, at least one input-output device and a system bus coupled to said memory interface unit, said system bus having a first grouping of address lines

coupled to address said system memory and a second grouping of address lines coupled to address said at least one input-output device.

8. A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said central processing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals.

9. The microprocessor system of claim 8 wherein said memory interface unit includes means for defining available time slots during which said system bus may be accessed, said available time slots being defined as being between accesses to said system bus by said IOP at said predetermined intervals.

10. The microprocessor system of claim 8 wherein said memory interface unit includes means for computing a bus access time required for one or more bus cycles involving said system bus, and for allocating one of said available time slots equal to or longer than said access time for execution of said one or more bus cycles.

11. The microprocessor system of claim 10 wherein said one or more bus cycles are memory cycles.

12. The microprocessor system of claim 11 in which the computation of said means for computing modifies the bus access time to provide sufficient time for input-output cycles.

13. In a microprocessor system having a microprocessing unit in which is included an arithmetic logic unit coupled to a stack cache, the improvement comprising:

means, coupled to said arithmetic logic unit and to said stack cache, for determining the availability of stack cache resources by determining whether a

value is included in at least one cell of said stack cache and whether at least one other cell of stack cache is empty; and

means, coupled to said means for determining the availability of said stack cache resources, for selectively inhibiting instruction execution by said arithmetic logic unit based on said availability of said stack cache resources.

14. The microprocessor system of claim 13 wherein said arithmetic logic unit includes means for executing instructions which generally push and pop only individual cells of said stack cache, said availability of stack cache resources being determined prior to initiating execution of each of said instructions.

15. In a microprocessor system having a microprocessing unit in which is included an arithmetic logic unit coupled to a stack cache, said stack cache being allocated at least a first portion of system memory, the improvement comprising:

means, coupled to said microprocessing unit and to said stack cache, for executing a stack management trap when a stack pointer of said stack cache assumes an address within a boundary region of said first portion of said system memory, said first stack management trap determining availability of at least one other portion of said system memory; and

means, coupled to said means for executing the stack management trap, for preventing another execution of said stack management trap until after said stack pointer has assumed an address within a predefined region of said first portion of said system not included within said boundary region.

16. A microprocessor system, comprising a microprocessing unit and a memory interface unit coupling said microprocessing unit to system random access memory (RAM), said microprocessor system including means, coupled to said memory interface unit, for converting logical row addresses provided by said microprocessing unit to physical row addresses of said system RAM so as to define virtual system memory using said system RAM.

17. The microprocessor system of claim 16 further including means, coupled to

said memory interface unit, for accessing said system RAM wherein each row address strobe (RAS) cycle includes a RAS precharge interval, said logical row addresses being converted to said physical addresses of said system RAM during said RAS precharge intervals.

18. A microprocessor system, comprising

a register unit, said register unit comprising at least one storage location containing a value to be interpreted as a memory address;

a memory interface unit coupled to said register unit;

a memory bus coupled to said memory interface unit; and

a system memory coupled to said memory interface unit by said memory bus;

said memory interface unit comprising transfer logic to increment said memory address and to generate a boundary detected signal when, after a memory bus transaction to said system memory using said memory address, said memory address after incrementing has a value that is an even multiple of 2^n, where n is a nonnegative integer.

19. The microprocessor system of claim 18 further comprising a microprocessing unit coupled to said memory interface unit and including means to interrupt said microprocessing unit after said boundary detected signal is generated by said memory interface unit.

20. The microprocessor system of claim 18 further comprising means coupled to said memory interface unit for generating a transfer request signal as an input to said memory interface unit for requesting said memory bus transaction to occur.

21. The microprocessor system of claim 20 further comprising an input-output processor (IOP) coupled to said memory interface unit, and said means for generating the transfer request signal is a means to execute instructions, one of said instructions activating said transfer request signal.

22. The microprocessor system of claim 18 wherein said incrementing of said memory address and the resulting said boundary detected signal is used to count an event.

23. The microprocessor system of claim 18 additionally comprising means coupled to said memory interface unit to disable said transfer logic to prevent further transfers after said boundary detected signal is generated.

24. The microprocessor system of claim 18 further comprising an input-output device coupled to said memory bus wherein said memory address is further comprised of a first grouping of address bits used to address said system memory and a second group of address bits used to address said input-output device.

25. In a microprocessor system including a central processing unit and a bit input register coupled to said central processing unit, said bit input register receiving logical input over at least one bit line, said bit input register comprising:

latch means, coupled to said at least one bit line, for initially sampling said at least one bit line in order to determine a logic level thereof; and

a zero persistence control unit, coupled to said latch means, for storing said logic level in a register assigned to said at least one bit line, said logic level remaining stored in said register until said zero persistence control unit is provided with a predefined signal by said central processing unit.

26. The microprocessor system of claim 25 further including a direct memory access controller (DMAC) coupled to said zero persistence controller, said DMAC including means for generating said predefined signal

27. A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), and a memory interface unit selectively coupling said central processing unit and said IOP to a system bus, said IOP including program counter means for providing system address information to said memory interface unit.

28. The microprocessor system of claim 27 further including means, coupled to said IOP and to said system bus, for granting said IOP access to said system bus at predetermined intervals.

29. The microprocessor system of claim 27 wherein said IOP includes latch means, coupled to said system bus, for latching data received from said system bus.

30. The microprocessor system of claim 27 wherein said IOP includes a multiplexer controlled by said program counter means, an instruction latch, and a decode/execute module, said multiplexer coupled between said instruction latch and said decode/execute module.

31. In a microprocessor system including a microprocessing unit having a stack cache, a system for effecting floating-point mathematical instructions comprising:

arithmetic logic unit means for performing floating-point operations upon values within cells of said stack cache;

means, coupled to said arithmetic logic unit means, for generating floating point exceptions in response to performance of selected ones of said floating point operations; and

mode register means, coupled to said arithmetic logic unit means and to said means for generating floating point exceptions, for enabling said microprocessing unit to execute predefined floating point routines in response to said floating point exceptions.

32. The system of claim 31 wherein said means for performing floating-point operations includes means, coupled to said stack cache, for executing test exponent, extract exponent, add exponents, and restore exponent instructions.

33. In a microprocessor system including a microprocessing unit having a stack cache, a method for executing a breakpoint instruction comprising the steps of:

pushing into said stack cache a memory address of said breakpoint

instruction; and

executing a breakpoint service routine.

34. In a microprocessor system including system memory and a microprocessing unit having one or more internal registers, said system memory being assigned a first address space for communication with said microprocessing unit, a method for transferring data within said microprocessing unit comprising the steps of:

assigning said one or more internal registers a second address space different from said first address space; and

transferring data to and from portions of said one or more internal registers identified by addresses within said second address space.

35. In a microprocessor system including a microprocessing unit having a stack cache, a method for address arithmetic comprising the steps of:

storing a first address value in a first cell of said stack cache;

storing a second address value in a second cell of said stack cache; and

adding said first address value to said second address value and storing a resultant sum value in said first cell of said stack cache.

36. In a microprocessor system including a microprocessing unit having a stack cache, a method for performing a copy byte operation comprising the steps of:

reading a least significant one of a plurality of data bytes stored in a cell;

replacing at least one other of said plurality of data bytes with said least significant data byte.

37. In a microprocessor system including a microprocessing unit having a stack cache and a carry register, a method for performing a test byte operation comprising the steps of:

reading each of a plurality of bytes stored within a cell of said stack cache; and

storing a first logical value in said carry register when any of said bytes are of zero value, and storing a second logical value in said carry register otherwise.

38. In a microprocessor system including a system memory, a microprocessing unit coupled to said system memory, having a stack cache coupled to said system memory and a program counter coupled to said stack cache, a single step processing system comprising:

means, coupled to said stack cache and to said program counter, for loading a first memory address from a first cell of said stack cache into said program counter;

means, coupled to said program counter, for executing a first instruction stored in said system memory of said microprocessor system at a location corresponding to said first memory address; and

means for executing a single-step trap routine during which a second memory address is loaded into said first cell wherein a second instruction following said first instruction is stored at a location in said system memory corresponding to said second memory address.

39. In a microprocessor system including system memory, and a microprocessing unit coupled to said system memory having a stack cache, a stack cache management system comprising:

means, coupled to said stack cache, for determining a number of cells currently included within said stack cache;

means, coupled to said means for determining the number of cells, for performing a comparison of said number of cells to a predefined depth of said stack cache; and

means, coupled to said means for performing the comparison, for providing an indication of a current stack depth based on said comparison.

40. In a microprocessor system including system memory, and a microprocessing unit coupled to said system memory having a stack cache, a stack cache management system comprising:

stack depth means, coupled to said stack cache, for determining a number of cells currently included within said stack cache; and

means, coupled to said stack depth means, for providing an indication of

said stack depth.

41. In a microprocessor system including system memory, and a microprocessing unit having a stack cache, a stack cache management system comprising:

means, coupled to said stack cache, for determining a current number cells in said stack cache;

means, coupled to said means for determining the current number of cells, for computing a number of cells capable of being added to said stack cache by comparing said current number of cells to a maximum stack depth; and

means, coupled to said stack cache and to said means for computing the number of cells capable of being added to said stack cache, for adding to said current number of cells in said stack cache a number of said cells equivalent to said number of cells capable of being added to said stack cache.

42. The system of claim 41 further including means, coupled to said stack cache, for removing from said current number of cells in said stack cache an additional number of said cells in said stack cache, and means for loading from said system memory into said stack cache said additional number of new cells.

43. A microprocessor comprising

a microprocessing unit that includes an arithmetic logic unit and a push-down stack coupled to said arithmetic logic unit,

said arithmetic logic unit including a bit-shifting means to shift bits, said bit shifting means shifting a count of bits in one or more partial shifts with said count reducing by the number of bits shifted each partial shift, said shifting being performed by multiple bits while said count is greater than said multiple, said multiple then being reduced, and then said shifting and said reductions of said count repeating until said count reaches zero.

44. The microprocessor of claim 43 wherein said multiple is initially eight and said multiple is reduced to one when said count is less than eight.